A CIRCUIT FOR A SELF-STROBED READING METHOD IN MAGNETIC DRUM DIGITAL STORES

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ABSTRACT A method that provides accurately timed output pulses that do not require clock pulses for their identification is described. The detailed circuit diagram used in association with the particular Magnetic Drum Memory is presented. The method is simple and elegant and is relatively insensitive to noise pulses in comparison with other methods.

INTRODUCTION

Well-known physical principles involved in audio recording on magnetic surface have offered a very successful method of storing digital data and instructions in all Information Processing systems (Booth, 1949). A comprehensive investigation was undertaken by one of the authors (Dutta Majumdar, 1959) on different aspects of design, development and applications of magnetic drum digital storage systems in this Laboratory (Electronics Research Laboratory of I.S.I.). The present circuit was designed, constructed and experimented with the magnetic drum store designed and built here (Dutta Majumdar, '61)

In drum stores it is customary to divide the magnetic surface into the cells each having a finite area. For recording binary information, the pulse currents of appropriate polarity are fed into a coil wound on a magnetic core which is almost magnetically complete except for a small airgap in the vicinity of the recording medium which is moved relative to this head. Either state of a binary digit is defined by the magnetic configuration of the cell. When the medium is moved relative to a pick-up head in close proximity of the digit cell, the fluxes associated with the digit cell will take up the minimum reluctance path along the pick-up head, and a voltage will be developed across the windings in the head approximately proportional to the time and space derivatives of the stored flux-pattern. The nature of the voltage wave form will give a clear indication of the state of magnetization of the medium. Different methods of recording and reproduction of digits are treated in text books (Booth, A.D., Wilkes, M. V. etc) in detail.

A Reading-Writting circuit for Return to Zero (RZ) method was described earlier (Dutta Majumdar, 1958) in connection with a track switching circuit. There the output of the read amplifier enters the strobing circuit where it is interpreted. That is, the read output wave form is examined at the second peak of

the differential flux waveform by means of a set of very sharp pulses called strobing pulses derived from clock pulses. In this paper a reading method and the corresponding circuit is described in which accurately timed output pulses are obtained that do not require clock-pulses for their identification

SELF-STROBED READING METHOD

The method consists in inverting and delaying the output waveform and then combining it with the original waveform in a gate or AND circuit In Fig. 1(a) the writing current waveform which is similar to that of RZ method is shown,

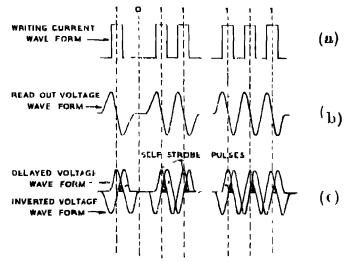


Fig 1 Self-strobed reading method.

and the corresponding output voltage waveform is indicated in Fig. 1(b). At this point it should be noted that the point at which the output signal crosses the axis from the positive to the negative side is an accurate indication of the location of the stored '1' In Fig. 1(c) the output waveform is duplicated twice, where it is shown after an inversion in one case and after a small amount of delay in the other case. If these waveforms are applied to an 'AND' gate that is responsive to voltage of positive polarity, sharp pulses as indicated by the darkened areas at the intersection of these two waveforms will be obtained. These pulses when properly amplified represent the stored binary information.

DESCRIPTION OF THE CIRCUIT

A functional block diagram of the circuit is shown in Fig. 2, and the actual circuit diagram is shown in Fig. 3. The output from the magnetic head is fed to

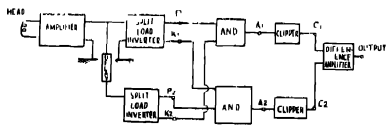


Fig. 2 Functional block diagram of the self-strobed reading method.

a conventional R-C coupled amplifier. The amplified output is fed to two split load inverters, one being fed direct, and the other through a delay line.

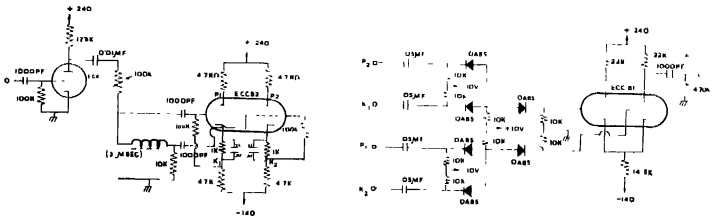


Fig. 3. Circuit diagram of the self-strobed reading circuit.

In this circuit the delay incorporated was about 3 MS which is about half the duration of the sharp central region of the head-output waveform. The inverters have equal loads on plate and cathode, so that we have at the four points, P_1,

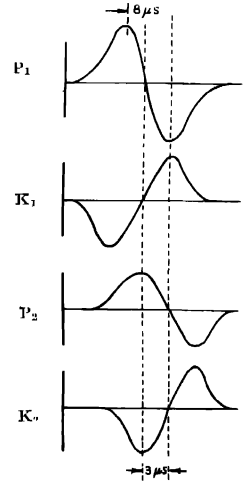


Fig. 4 Waveform, Direct, Inverted, Delayed direct and Delayed Inverted.

K_1, P_2, K_2, waveforms which are respectively direct, inverted, delayed direct and delayed inverted replicas of the head output waveform (Fig. 4). The outputs from P_1 and K_2, and P_2 and K_1 are respectively fed to two AND gates (which are OR gates for negative inputs). The resulting outputs form the two gates are applied to two diode limiters which block the -ve parts of the incoming signal and pass only the positive parts. The outputs of the limiters are fed to the two grids of a difference amplifier At the output of the difference amplifier, with this circuit arrangement sharp positive pulses for "1" and sharp

negative pulses for "0" are obtained (Fig. 5 two photographs are shown.) If instead of two channels before the 'AND' gates only one channel is used, there can be only sharp self-strobed positive pulses for '1's, whereas those for '0' s will be

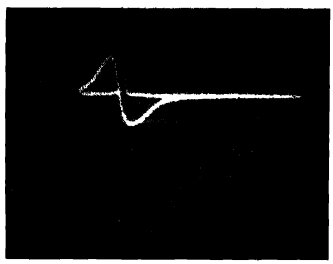
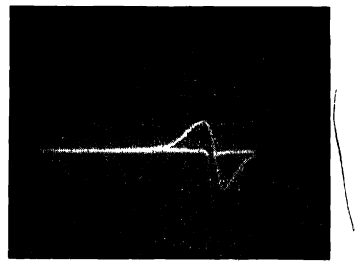


Fig. 5(a) self-strobed sharp positive pulse for a "one".



(b) sharp negative pulse for a "Zero".

absent. The present circuit was designed for the particular head output pulse amplitude (about 0.75 volts), and for a particular Drum Speed (about 6000 r.p.m.). With the variation of these and other requirements the circuit constants will be different, but the general scheme can remain same. By selecting the delay and the associated circuit constants a compromise is to be made between the amplitude of the signal through the gate and the accuracy in locating the cross over point. Another advantage of this sensing method is its relative insensivity to noise pulses.

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REFERENCES

Booth, A. D., July, 1949, *Electronic Engineering.*
Booth, A. D, and Booth, K, Automatic Digital Calculators.
Dutta Majumdar, D., Dec. 1958, *Electronic Engineering*, 702-5.
Dutta Majumdar, D., 1959, *J. Inst. Telecom. Engineers.*, **5**, **4**, 211-22.
Dutta Majumdar, D., 1961, *J. Inst., Telecom. Engineers.*, **7**, **1**, 27-36.
Wilkes, M. V., Automatic Dogital Computers.